EAST SEARCH

11/14/02

L#	Hits	Search String	Databases
L1	1	value change dump and (session with (range or length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	12080	simulat$3 with (range or length or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	575	simulat$3 with (target with (range or length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	1	value change dump and (simulat$3 with (session with (range or length or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	1	value change dump and (simulat$3 with (target with (range or length or duration)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	28	simulation history	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	1	(simulat$3 with (target with (range or length or duration))) and "simulation history"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	1	(simulat$3 with (session with (range or length or duration))) and "simulation	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	1	value change dump and "simulation history"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	28	value change dump	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	14	simulat$3 with (session with (range or length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	194	simulat$3 with (interval with (range or length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	0	value change dump with (interval or length or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	1	value change dump same (interval or length or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	9999	integrated circuit with testing	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	909	("integrated circuit" with testing) and (test with (interval or length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	0	(("integrated circuit" with testing) and (test with (interval or length or duration))) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	9	(("integrated circuit" with testing) and (test with (interval or length or duration))) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L22	3	record with "simulation history"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L23	0	("value change dump" or VCD) with "on demand"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L24	2	6,370,494.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L25	1	6,370,494.pn. and (interval or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L26	176	simulat$3 with (target with (length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L27	0	circuit simulation with "reconfigurable hardware"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L28	210	reconfigurable hardware	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L29	0	reconfigurable hardware same "circuit simulation"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L30	23	reconfigurable hardware same "circuit design"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L31	417	(system or hardware) with states with interval$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	1	(system or hardware) with states with interval$1 same save	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L33	5	(system or hardware) with states with interval$1 with (determine or compute)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L32	0	simulat$3 with ((subinterval or subrange) with (length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	1	test$3 with ((subinterval or subrange) with (length or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	(co-simulation with ("virtual time" or "time frame")) same message-log$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	co-simulation with ("virtual time" or "time frame")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	cosimulation with ("virtual time" or "time frame")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	cosimulation same ("virtual time" or "time frame")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

0	cosimulation with message-log$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
2	damini.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
0	damini.in. and (interval or duration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
528	garg.in. or garj.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
6	(garg.in. or garj.in.) and ((simulat$3 or test$3) with (interval or lenght or duration))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
12	(garg.in. or garj.in.) and ((simulat$3 or test$3) with (range))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
3	Simulat$ same STIL	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
1	Simulat$ same "Standard Test Interface language"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

09/373,014 **Ping-sheng Tseng et al.**

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11/14/02

Results of search set L16: robotic adj (controller or "control system") and (sens$2 with (variables or signals))

Document)ocument II	Title	Source	Issue Date	Current OR	Abstract
US 20020152060 A1	Inter-chip communication system		20021017	703/17	
US 20020138809 A1	Multi-level power macromodeling		20020926	716/1	
US 20020108094 A1	System and method for designing integrated circuits		20020808	716/5	
US 20020059054 A1	Method and system for virtual prototyping		20020516	703/20	
US 20020040288 A1	Method for design validation of complex IC		20020404	703/17	
US 20020004919 A1	Method for locating functional mistakes in digital circuit designs		20020110	714/39	
US 20020002698 A1	Method for verifying the design of a microprocessor		20020103	716/4	
US 6449751 B1	Method of analyzing static current test vectors with reduced file sizes for semiconductor integrated circuits		20020910	716/4	
US 6421251 B1	Array board interconnect system and method		20020716	361/788	
US 6389379 B1	Converification system and method		20020514	703/14	
US 6370675 B1	Semiconductor integrated circuit design and evaluation system using cycle base timing		20020409	716/6	
US 6363509 B1	Method and apparatus for transforming system simulation tests to test patterns for IC testers		20020326	714/738	
US 6321366 B1	Timing-insensitive glitch-free logic system and method		20011120	716/6	
US 6292765 B1	Method for automatically searching for functional defects in a description of a circuit		20010918	703/14	
US 6249891 B1	High speed test pattern evaluation apparatus		20010619	714/738	
US 6134516 A	Simulation server system and method		20001017	703/27	
US 6083269 A	Digital integrated circuit design system and methodology with hardware		20000704	703/14	
US 6061511 A	Reconstruction engine for a hardware circuit emulator		20000509	703/28	
US 6061283 A	Semiconductor integrated circuit evaluation system		20000509	365/201	
US 6026230 A	Memory simulation system and method		20000215	703/13	
US 6009256 A	Simulation/emulation system and method		19991228	703/13	
US 5889685 A	Method and apparatus for automatically characterizing short circuit current and power consumption in a digi		19990330	703/18	
US 5838947 A	Modeling, characterization and simulation of integrated circuit power behavior		19981117	703/14	
US 5835380 A	Simulation based extractor of expected waveforms for gate-level power analysis tool		19981110	716/2	
US 5768145 A	Parametrized waveform processor for gate-level power analysis tool		19980616	703/14	

US 5633879 A	Method for integrated circuit design and test	19970527 714/738
JP 2001349928 A	SEMICONDUCTOR TEST SYSTEM	20011221
JP 2001349928 A	Semiconductor device testing system e.g. for digital LSI, converts format of data output by test device, into \	20011221